CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) A method comprising: receiving a packet at a network device; pre-fetching a protocol control block (PCB) associated with the packet into a cache of a selected processing unit; queuing the packet for processing; pre-fetching a header associated with the packet into the cache of the selected processing unit; and retrieving the PCB from the cache of the selected processing unit when [a] the selected processing unit is ready to process the packet.

2. (currently amended) The method of claim 1, further comprising checking the destination of the interrupt and disabling interrupts from a network interface. ~~further comprising pre-fetching a header associated with the packet into the cache.~~

3. (currently amended) The method of claim 2, further comprising retrieving the packet header from the cache associated with the selected processing unit when the processing unit is ready to process the packet.

4. (original) The method of claim 1, further comprising sending an interrupt to notify the selected processing unit of the receipt of the packet.

5. (currently amended) The method of claim 4, wherein the interrupt is a software interrupt. ~~1, wherein pre-fetching a PCB associated with the packet into a cache comprises pre-fetching a PCB associated with the packet into a cache of the processing unit.~~

6. (original) The method of claim 5, further comprising storing the packet in a memory coupled to the processing unit.

7. (original) The method of claim 1, further comprising processing the packet.

8. (currently amended) An apparatus comprising: a receive unit to receive a packet; a pre-fetch unit coupled to the receive unit to pre-fetch a protocol control block (PCB) associated with the packet and a header associated with the packet into a cache of a processing unit and queue the packet processing; and [a] the processing unit coupled to the pre-fetch unit to retrieve the PCB and the header from the cache and process the packet.

9. (original) The apparatus of claim 8, wherein the receive unit is a network interface card.

10. (currently amended) The apparatus of claim [8] 9, further comprising an interrupt service unit to check the destination of the interrupt, disable further interrupts from the network interface card, initiate a software interrupt, and queue the packet for processing. ~~wherein the pre-fetch unit to further pre-fetch a header associated with the packet into the cache.~~

11. (canceled).

12. (canceled).

13. (original) The apparatus of claim 8, further comprising an interrupt unit coupled to the receive unit and the processing unit to receive an interrupt from the receive unit and notify the processing unit of the packet.

14. (currently amended) An article of manufacture comprising: a machine accessible medium including content that when accessed by a machine causes the machine to: receive a packet; pre-fetch a protocol control block (PCB) associated with the packet and a header associated with the packet into a cache of a processing unit; queue the packet for processing; and retrieve the PCB from the cache when [a] the processing unit is ready to process the packet.

15. (currently amended) The article of manufacture of claim 14, wherein the machine-accessible medium further includes content that causes the machine to pre-fetch [a] the header associated with the packet into the cache.

16. (original) The article of manufacture of claim 15, wherein the machine-accessible medium further includes content that causes the machine to retrieve the packet header from the cache when the processing unit is ready to process the packet.

17. (original) The article of manufacture of claim 14, wherein the machine-accessible medium further includes content that causes the machine to process the packet.

18. (original) The article of manufacture of claim 14, wherein the machine- accessible medium further includes content that causes the machine to send an interrupt to notify the processing unit of the receipt of the packet.

19. (canceled)

20. (original) The article of manufacture of claim 14, wherein the machine accessible medium further includes content that causes the machine to store the packet in a memory coupled to the processing unit.

21. (currently amended) A system comprising: a receive unit to receive a packet; a memory coupled to the receive unit to store the received packet; a memory controller coupled to the memory to manage the memory; a pre-fetch unit coupled to the receive unit to pre-fetch a protocol control block (PCB) associated with the packet and a header associated with the packet into a cache of a processor and queue the packet for processing; and a processing unit to retrieve the PCB from the cache of the processor and process the packet.

22. (original) The system of claim 21, wherein the receive unit is a network interface card.

23. (canceled)

24. (currently amended) The system of claim [23] 21, wherein the processing unit to further retrieve the packet header from the cache.

25. (original) The system of claim 21, further comprising an interrupt unit coupled to the receive unit and the processing unit to receive an interrupt from the receive unit and notify the processing unit of the packet.